



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Reithinger, *et al.*

Attorney Docket: 00P7685US

Filed: June 16, 2000

Examiner: Phat X. Cao

Serial No.: 09/596,129

Art Unit: 2814

For: Multiple Chip Semiconductor Arrangement having Electrical Components in Separating Regions

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Respectfully submitted,


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January 19, 2004

Date

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PTO/SB/08A (05-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				C <i>mpl te if Known</i>	
Sheet	1	of	1	Application Number	09/596,129
				Filing Date	June 16, 2000
				First Named Inventor	Reithinger, et al.
				Art Unit	2814
				Examiner Name	Phat X Cao
				Attorney Docket Number	00P7685US

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
	2	JP-01-220843	09-04-1989	NEC Corp.	English Abstract only	
	3	JP-63-234553	09-29-1988	NEC Corp.	English Abstract only	
	4	JP-04-171860	06-19-1992	Hitachi Ltd.	English Abstract only	
	5	JP-11-163062	06-18-1999	Toshiba Corp.	English Abstract only	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

CITATION FOR ART. OR NON-ART. LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

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